HCS410

KEELOQ Code Hopping Encoder and Transponder*

FEATURES

Security

- Two programmable 64-bit encoder keys
- 16/32-bit bi-directional challenge and response using one of two keys
- 69-bit transmission length
- 32-bit unidirectional code hopping, 37-bit nonencrypted portion
- · Encoder keys are read protected
- Programmable 28/32-bit serial number
- 60-bit, read-protected seed used for secure learning
- · Three IFF encryption algorithms
- · Delayed increment mechanism
- · Asynchronous transponder communication
- · Queuing information transmitted

Operating

- 2.0V to 6.6V operation, 13V encoder only operation
- Three switch inputs [S2, S1, S0]—seven functions
- Batteryless bi-directional transponder
- Selectable baud rate and code word blanking
- · Automatic code word completion
- · Battery low signal transmitted
- · Nonvolatile synchronization
- PWM or Manchester RF encoding
- · Combined transmitter, transponder operation
- Anti-collision of multiple transponders
- Passive proximity activation
- · Device protected against reverse battery

Other

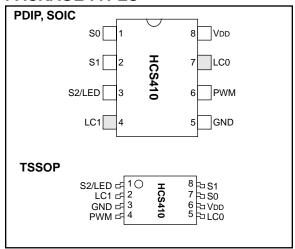
- 37-bit nonencrypted part contains 28/32-bit serial number, 4/0-bit function code, 1-bit battery low, 2-bit CRC, 2-bit queue
- · Easy to use programming interface
- On-chip tunable RC oscillator (±10%)
- On-chip EEPROM
- 64-bit user EEPROM in transponder mode
- · Battery-low LED indication
- SQTP serialization guick-time programming
- 8-pin PDIP/SOIC/TSSOP and die

Typical Applications

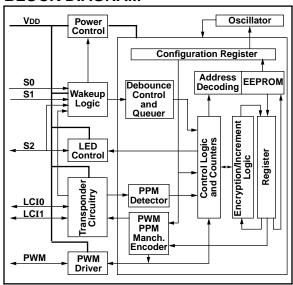
- · Automotive remote entry systems
- Automotive alarm systems
- · Automotive immobilizers
- Gate and garage openers
- Electronic door locks (Home/Office/Hotel)
- · Burglar alarm systems
- · Proximity access control

KEELOQ is a registered trademark of Microchip Technology Inc.
*Code hopping encoder patents issued in Europe, U.S.A., R.S.A.—U.S.A.: 5,517,187; Europe: 0459781

PACKAGE TYPES



BLOCK DIAGRAM



DESCRIPTION

The HCS410 is a code hopping transponder device designed for secure entry systems. The HCS410 utilizes the patented KEELOQ code hopping system and bidirectional challenge-and-response for logical and physical access control. High security learning mechanisms make this a turnkey solution when used with the KEELOQ decoders. The encoder keys and synchronization information are stored in protected on-chip EEPROM.

A low cost batteryless transponder can be implemented with the addition of an inductor and two capacitors. A packaged module including the inductor and capacitor will also be offered.

A single HCS410 can be used as an encoder for Remote Keyless Entry (RKE) and a transponder for immobilization in the same circuit and thereby dramatically reducing the cost of hybrid transmitter/transponder circuits.

1.0 SYSTEM OVERVIEW

1.1 Key Terms

- <u>CH Mode</u> Code Hopping Mode. The HCS410 will transmit a 69-bit transmission each time it is activated, with at least 32-bits changing each time the encoder is activated.
- Encoder Key A unique 64-bit key generated and programmed into the encoder during the manufacturing process. The encoder key controls the encryption algorithm and is stored in EEPROM on the encoder device.
- IFF Identify friend or foe is a means of validating a token. A decoder will send a random challenge to the token and check that the response of the token is a valid response.
- KEELOQ Encryption Algorithm The high security level of the HCS410 is based on the patented KEELOQ technology. A block cipher encryption algorithm based on a block length of 32 bits and a key length of 64 bits is used. The algorithm obscures the information in such a way that even if the unencrypted/challenge information differs by only one bit from the information in the previous transmission/challenge, the next coded transmission/response will be totally different. Statistically, if only one bit in the 32-bit string of information changes, approximately 50 percent of the coded transmission will change.
- <u>Learn</u> The HCS product family facilitates several learning strategies to be implemented on the decoder. The following are examples of what can be done.

Normal Learn –The receiver uses the same information that is transmitted during normal operation to derive the transmitter's encoder key, decrypt the discrimination value and the synchronization counter.

Secure Learn* – The transmitter is activated through a special button combination to transmit a stored 60-bit value (random seed) that can be used for key generation or be part of the key. Transmission of the random seed can be disabled after learning is completed.

 Manufacturer's Code – A 64-bit word, unique to each manufacturer, used to produce a unique encoder key in each transmitter (encoder).

^{*}Secure Learn patent pending.

1.2 KEELoQ Code Hopping Encoders

When the HCS410 is used as a code hopping encoder device, it is ideally suited to keyless entry systems, primarily for vehicles and home garage door openers. It is meant to be a cost-effective, yet secure solution to such systems. The encoder portion of a keyless entry system is meant to be held by the user and operated to gain access to a vehicle or restricted area.

Most keyless entry systems transmit the same code from a transmitter every time a button is pushed. The relative number of code combinations for a low end system is also a relatively small number. These shortcomings provide the means for a sophisticated thief to create a device that 'grabs' a transmission and retransmits it later or a device that scans all possible combinations until the correct one is found.

The HCS410 employs the KEELOQ code hopping technology and an encryption algorithm to achieve a high level of security. Code hopping is a method by which the code transmitted from the transmitter to the receiver is different every time a button is pushed. This method, coupled with a transmission length of 69 bits, virtually eliminates the use of code 'grabbing' or code 'scanning'.

The HCS410 has a small EEPROM array which must be loaded with several parameters before use. The most important of these values are:

- A 28/32-bit serial number which is meant to be unique for every encoder
- · 60-bit seed value
- A 64-bit encoder key that is generated at the time of production
- A 16-bit synchronization counter value.
- · Configuration options

The 16-bit synchronization counter value is the basis for the transmitted code changing for each transmission, and is updated each time a button is pressed. Because of the complexity of the code hopping encryption algorithm, a change in one bit of the synchronization counter value will result in a large change in the actual transmitted code. Once the encoder detects that a button has been pressed, the encoder reads the button and updates the synchronization counter. The synchronization counter value, the function bits, and the discrimination value are then combined with the encoder key in the encryption algorithm, and the output is 32 bits of encrypted information (Figure 1-1). The code hopping portion provides up to four billion changing code combinations. This data will change with every button press, hence, it is referred to as the code hopping portion of the code word.

The 32-bit code hopping portion is combined with the button information and the serial number to form the code word transmitted to the receiver. The code word format is explained in detail in Section 2.1.

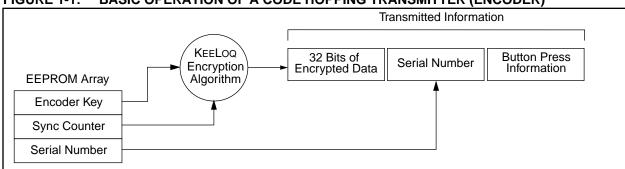


FIGURE 1-1: BASIC OPERATION OF A CODE HOPPING TRANSMITTER (ENCODER)

© 1997 Microchip Technology Inc.

Preliminary

DS40158B-page 3

1.3 KEELOQ IFF

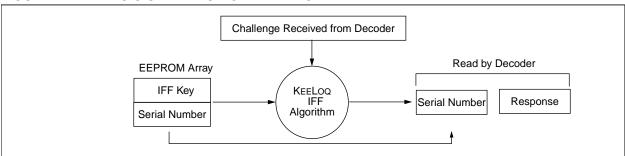
The HCS410 can be used as an IFF transponder for verification of a token. In IFF mode the HCS410 is ideally suited for authentication of a key before disarming a vehicle immobilizer. Once the key has been inserted in the car's ignition the decoder would inductively poll the key validating it before disarming the immobilizer.

IFF validation of the token involves a random challenge being sent by a decoder to a token. The token then generates a response to the challenge and sends this response to the decoder (Figure 1-2). The decoder calculates an expected response using the same challenge. The expected response is compared to the response received from the token. If the responses match, the token is identified as a valid token and the decoder can take appropriate action.

The HCS410 can do either 16 or 32-bit IFF. The HCS410 has two encryption algorithms that can be used to generate a response to a challenge. In addition there are up to two encoder keys that can be used by the HCS410. Typically each HCS410 will be programmed with a unique encoder key(s).

In IFF mode, the HCS410 will wait for a command from the base station and respond to the command. The command can either request a read/write from user EEPROM or an IFF challenge response. A given 16 or 32-bit challenge will produce a unique 16/32-bit response, based on the IFF key and IFF algorithm used.

FIGURE 1-2: IBASIC OPERATION OF AN IFF TOKEN



2.0 DEVICE OPERATION

The HCS410 can either operate as a normal code hopping transmitter with one or two IFF keys (Figure 2-1) or as purely an IFF token with two IFF keys (Figure 2-2 and Figure 2-3). When used as a code hopping transmitter the HCS410 only needs the addition of buttons and RF circuitry for use as a transmitter. Adding the transponder function to the transmitter requires the addition of an inductor and two capacitors as shown in Figure 2-1 and Figure 2-2. A description of each pin is given in Table 2-1. Table 2-2 shows the function codes for using the HCS410.

FIGURE 2-1: COMBINED TRANSMITTER/ TRANSPONDER CIRCUIT

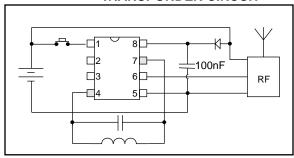


FIGURE 2-2: TRANSPONDER CIRCUIT

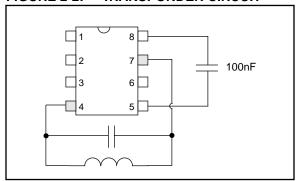


FIGURE 2-3: 2-WIRE, 1 OR 2-KEY IFF TOKEN

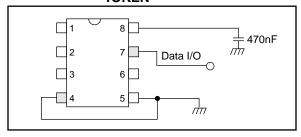


FIGURE 2-4: HCS410 ENCODER WITH 12V BATTERY

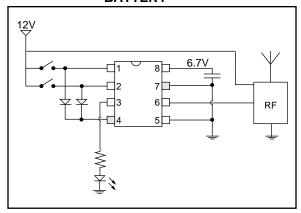


FIGURE 2-5: LED CONNECTION TO S2/LED OUTPUT

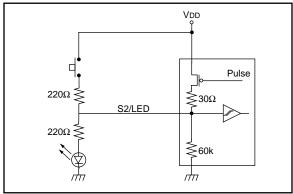
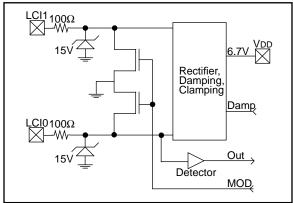


FIGURE 2-6: LC PIN BLOCK DIAGRAM



HCS410

TABLE 2-1: PINOUT DESCRIPTION

Name	Pin Number	Description
S0	1	Switch input 0
S1	2	Switch input 1
S2/LED	3	Switch input 2/LED output, Clock pin for programming mode
LC1	4	Transponder interface pin
Vss	5	Ground reference connection
PWM	6	Pulse width modulation (PWM) output pin/Data pin for programming mode
LC0	7	Transponder interface pin.
VDD	8	Positive supply voltage connection

TABLE 2-2: FUNCTION CODES

	LC1	LC0	S2	S1	S0	Comments
1	0	0	0	0	1	Normal Code Hopping transmission
2	0	0	0	1	0	Normal Code Hopping transmission
3	0	0	0	1	1	Delayed seed transmission if allowed by SEED and TMPSD/ Normal Code Hopping transmission
4	0	0	1	0	0	Normal Code Hopping transmission
5	0	0	1	0	1	Normal Code Hopping transmission
6	0	0	1	1	0	Normal Code Hopping transmission
7	0	0	1	1	1	Immediate seed transmission if allowed by SEED and TMPSD/ Normal Code Hopping transmission
8	1/0	0/1	0	0	0	Transponder mode

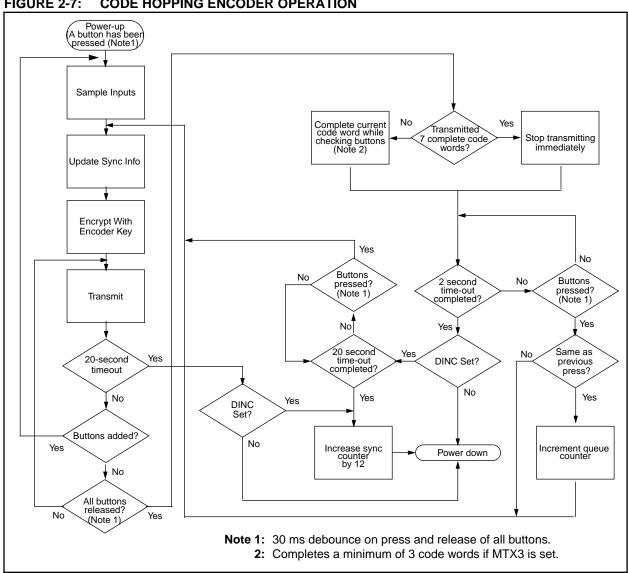
2.1 **Code Hopping Mode (CH Mode)**

The HCS410 will wake up upon detecting a switch closure and then delay approximately 30 ms for switch debounce (Figure 2-7). The synchronization counter value, fixed information, and switch information will be encrypted to form the code hopping portion. The encrypted or code hopping portion of the transmission will change every time a button is pressed, even if the same button is pushed again. Keeping a button pressed for a long time will result in the same code word being transmitted until the button is released or time-out occurs. A code that has been transmitted will not occur again for more than 64K transmissions. Overflow information programmed into the encoder can be used by the decoder to extend the number of unique transmissions to more than 192k.

If, in the transmit, process it is detected that a new button(s) has been added, a reset will immediately be forced and the code word will not be completed. Please note that buttons removed will not have any effect on the code word unless no buttons remain pressed in which case the current code word will be completed and the power down will occur. If, after the button is pressed, the button is pressed again within 2 seconds, the current transmission will be aborted and a new transmission will start with the QUE counter incremented.

Note: When used in Code Hopping Mode (CH Mode), the HCS410 can also be used as an IFF token.

CODE HOPPING ENCODER OPERATION



2.1.1 TRANSMISSION FORMAT

The HCS410 transmission (CH Mode) is made up of several parts (Figure 2-10 and Figure 2-12). Each transmission is begun with a preamble and a header, followed by the encrypted and then the fixed data. The actual data is 69 bits which consists of 32 bits of encrypted data and 37 bits of fixed data. Each transmission is followed by a guard period before another transmission can begin. Refer to Table 5-4 and Table 5-5 for transmission timing specifications. The combined encrypted and nonencrypted sections increase the number of combinations to 1.47 x 10²⁰.

The HCS410 transmits a 69-bit code word when a button is pressed. The 69-bit word is constructed from a Fixed Code portion and an Code Hopping portion (Figure 2-8).

The **Encrypted Data** is generated from 4 function bits, 2 overflow bits, and 10 discrimination bits, and the 16-bit synchronization counter value (Figure 2-8).

The **Nonencrypted Code Data** is made up of 2 QUE bits, 2 CRC bits, a VLow bit, 4 function bits, and the 28-bit serial number. If the extended serial number (32 bits) is selected, the 4 function code bits will not be transmitted (Figure 2-8).

FIGURE 2-8: HOP CODE WORD ORGANIZATION (RIGHT-MOST BIT IS CLOCKED OUT FIRST)

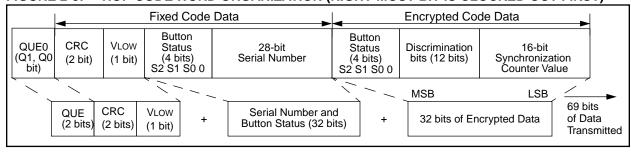


FIGURE 2-9: SEED CODE WORD ORGANIZATION

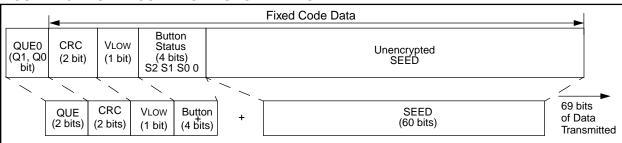
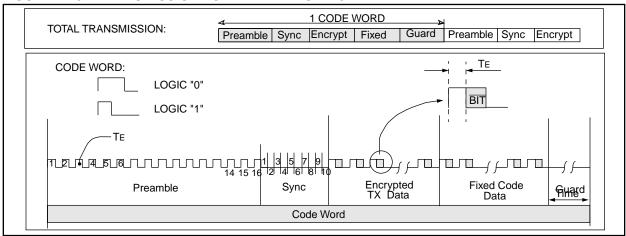


FIGURE 2-10: TRANSMISSION FORMAT—MANCH = 0



2.2 <u>Code Hopping Mode Special Features</u>

2.2.1 CODE WORD COMPLETION

Code word completion is an automatic feature that ensures that the entire code word is transmitted, even if the button is released before the transmission is complete. The HCS410 encoder powers itself up when a button is pushed and powers itself down after the command is finished (Figure 2-7). If the button is held down beyond the time for one transmission, then multiple transmissions will result. If another button is added during a transmission, the active transmission will be aborted and the new code will be generated using the new button information. If MTX3 is set in the configuration word, a minimum of three transmissions will be transmitted when the HCS410 is activated, even if the buttons are released.

If less than seven words have been transmitted when the buttons are released, the HCS410 will complete the current word. If more than seven words have been transmitted, and the button is released, the PWM output is immediately switched off.

2.2.2 CODE WORD BLANKING ENABLE

Federal Communications Commission (FCC) part 15 rules specify the limits on fundamental power and harmonics that can be transmitted. Power is calculated on the worst case average power transmitted in a 100ms window. It is therefore advantageous to minimize the duty cycle of the transmitted word. This can be achieved by minimizing the duty cycle of the individual bits and by blanking out consecutive words. Code Word Blanking Enable (CWBE) is used for reducing the average power of a transmission (Figure 2-11). Using the CWBE allows the user to transmit a higher amplitude transmission if the transmission length is shorter. The FCC puts constraints on the average power that can be transmitted by a device, and CWBE effectively prevents continuous transmission by only allowing the transmission of every second or fourth word. This reduces the average power transmitted and hence, assists in FCC approval of a transmitter device.

The HCS410 will either transmit all code words, 1 in 2 or 1 in 4 code words, depending on the baud rate selected. See Section 3.7 for additional details.

CWBE Disabled
(All words transmitted)

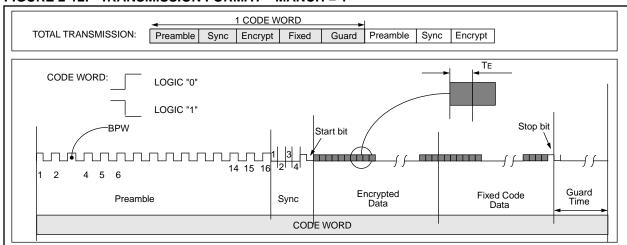
CWBE Enabled
(1 out of 2 transmitted)

CWBE Enabled
(1 out of 4 transmitted)

Time

FIGURE 2-11: CODE WORD BLANKING ENABLE

FIGURE 2-12: TRANSMISSION FORMAT—MANCH = 1



2.2.3 CRC (CYCLE REDUNDANCY CHECK) BITS

The CRC bits are calculated on the 65 previously transmitted bits. The CRC bits can be used by the receiver to check the data integrity before processing starts. The CRC can detect all single bit and 66% of double bit errors. The CRC is computed as follows:

EQUATION 2-1: CRC CALCULATION

$$CRC[1]_{n+1} = CRC[0]_n \oplus Di_n$$

and

$$CRC[0]_{n+1} = (CRC[0]_n \oplus Di_n) \oplus CRC[1]_n$$

with

$$CRC[1,0]_0 = 0$$

and Di_n the nth transmission bit $0 \le n \le 64$

2.2.4 SEED TRANSMISSION

In order to increase the level of security in a system, it is possible for the receiver to implement what is known as a secure learning function. This can be done by utilizing the seed value on the HCS410 which is stored in EEPROM. Instead of the normal key generation method being used to create the encoder key, this seed value is used and there should not be any mathematical relationship between serial numbers and seeds for the best security. See Section 3.7.3 for additional details.

2.2.5 PASSIVE PROXIMITY ACTIVATION

If the HCS410 is brought into a magnetic field it will enter IFF mode. In this mode it will send out ACK pulses on the LC lines. If the HCS410 doesn't receive any response to the ack pulses within 100ms the HCS410 will transmit a normal code hopping transmission for 2 seconds if XPRF is set in the configuration word. The function code during this transmission is S2:S0 = 000.

2.2.6 AUTO-SHUTOFF

The Auto-shutoff function automatically stops the device from transmitting if a button inadvertently gets pressed for a long period of time. This will prevent the device from draining the battery if a button gets pressed while the transmitter is in a pocket or purse. Time-out period is approximately 20 seconds.

2.2.7 VLow: VOLTAGE LOW INDICATOR

The VLow bit is transmitted with every transmission (Figure 2-12 operating voltage has dropped below the low voltage trip point, approximately 2.2V or 3.8V selectable at 25°C. This VLow signal is transmitted so the receiver can give an indication to the user that the transmitter battery is low.

2.2.8 QUE0:QUE1: QUEUING INFORMATION

If a button is pressed, released for more than 60 ms, and pressed again within 2 seconds the QUE counter is incremented (Figure 2-7). The transmission that the HCS410 is busy with is aborted and a new transmission is begun with the new QUE bits set. These bits can be used by the decoder to perform secondary functions using only a single button but without the requirement that the decoder receive more than one completed transmission. For example if none of the QUE bits are set the decoder only unlocks the driver's door, if QUE0 is set (double press on the transmitter) the decoder unlocks all the doors.

Note: The QUE will not overflow.

2.2.9 OTHER CONFIGURABLE OPTIONS

Other configurable code hopping options include an

- · LED output enable
- Transmission-rate selection
- Extended serial number.

These are described in more detail in Section 3.7.

2.3 IFF Mode

IFF mode allows the decoder to perform an IFF validation, to write to the user EEPROM and to read from the user EEPROM. Each operation consists of the decoder sending an opcode data and the HCS410 giving a response.

There are two IFF modes: IFF1 and IFF2. IFF1 allows only one key IFF, while IFF2 allows two keys to be used.

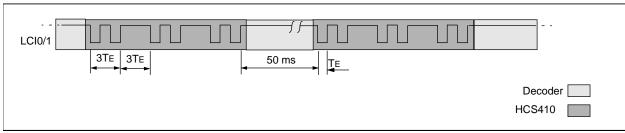
Note: When IFF 2 is enabled, seed transmissions will not be allowed.

It is possible to use the HCS410 as an IFF token without using a magnetic field for coupling. The HCS410 can be directly connected to the data line of the decoder as shown in Figure 2-3. The HCS410 gets its power from the data line as it would in normal transponder mode. The communication is identical to the communication used in transponder mode.

2.3.1 IFF MODE ACTIVATION

The HCS410 will enter IFF mode if the capacitor/inductor resonant circuit generates a voltage greater than approximately 3.0 volts on LC0 or LC1. After the verified application of power and elapse of the normal reset period, the device will start responding by pulsing the DATA line with a string of marker pulses as shown in Figure 2-13. This action will continue until the pulse train is terminated by receiving a start signal of duration 2TE, on the LC inputs before the next expected marker pulse. The device now enters the IFF mode and expects to receive an 'Opcode' and a 0/16/32-bit Datastream to react on. The data rate (TE) is determined by the BSL bits in the configuration word. See Section 3.0 for additional detail.

FIGURE 2-13: IFF MODE ACTIVATION



Patents have been applied for.

2.3.2 IFF DECODER COMMANDS

As shown in Figure 2-14, a logic 1 and 0 are differentiated by the time between two rising edges. A long pulse indicates a 1; a short pulse, a 0.

FIGURE 2-14: MODULATION FOR IFF COMMUNICATION

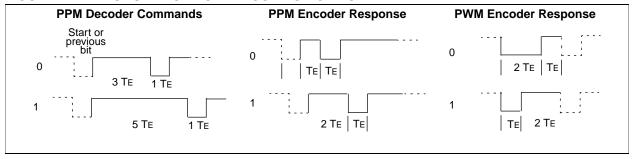


FIGURE 2-15: OVERVIEW OF IFF OPERATION

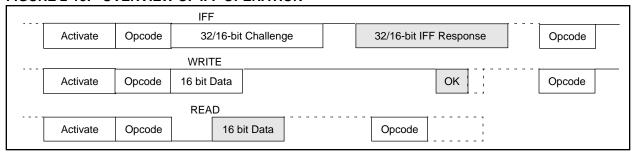


FIGURE 2-16: DECODER IFF COMMANDS AND WAVEFORMS

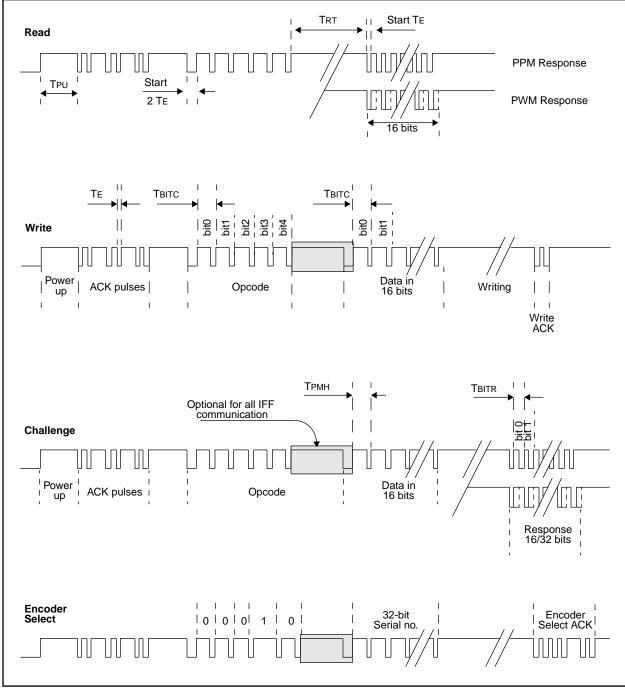


TABLE 2-3: IFF TIMING

Parameter		Symbol	Min.	Typical	Max.	Units	Comments
Basic Time Element	BSL≠3	TE	180	90	200		(Note 1)
	BSL = 3	IE	90	100	110	μs	(Note 1)
Power up Time		Tpu	32	36.5	41	ms	(Note 1)
PPM Command bit Time	Data = 0	Твітс	3.5	4	4.5	TE	
	Data = 1	IBIIC	5.5	6	6.5	16	
PPM Response bit Time	Data = 0	Твітк	1.8	2	2.7	TE	
	Data = 1	IBIIK	2.7	3	3.3	16	
PPM Command Minimum High Time		ТРМН	1.5			TE	
Response Time		Trt	6.5			ms	(Note 2)
Opcode to Data input delay	Note 3	Totd	1.5			ms	(Note 3)

Note 1: Values with Ocscillator trimmed.

- 2: Fastest for read.
- 3: The opcode and data input can be transmitted as one data stream, except during programming where a minimum of 2.2 ms should be allowed.

2.3.3 HCS410 RESPONSES

The responses from the HCS410 have either PWM format or PPM format, depending on the status of the PPM bit in the configuration word. See Figure 2-13 for additional information

2.3.4 IFF CHALLENGE RESPONSE

The 16/32 bit response, to a 16/32 bit challenge, will be transmitted once, after which, the device will be ready to accept another command until removal of power. The same applies to the result of a Read command. The opcode written to the device specifies the challenge length and algorithm used.

2.3.5 IFF WRITE

The decoder can write to USER[0:3], SER[0:1], and the configuration word in the EEPROM. When in IFF1 mode the HCS410 will write protect SER0 and SER1 as these positions contain the serial number transmitted in CH Mode.

After the HCS410 has written the word into the EEPROM, it will give two acknowledge pulses (TE wide and TE apart) on the LC pins.

Note: If the configuration word is written, the device needs to be reset to allow the new configuration settings to come into effect.

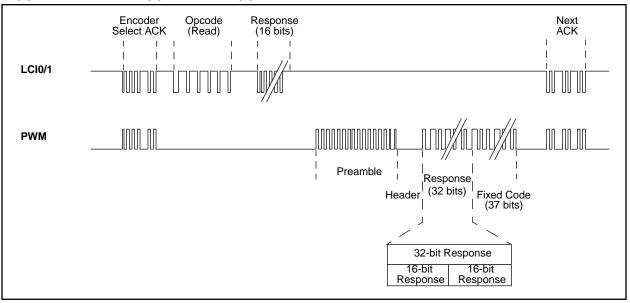
2.3.6 IFF READ

The decoder can read USER[0:3], SER[0:1], and the configuration word in the EEPROM. After the data has been read, the device is ready to receive a command again.

2.3.7 IFF PROGRAMMING

Upon receiving a programming opcode, the EEPROM is erased. Thereafter, the first 16 bits of data can be written. After indicating that a write command has been successfully completed the device is ready to receive the next 16 bits. After a complete memory map was received. it will be transmitted in PWM format on the LC pins. This enables wireless programming of the device.

FIGURE 2-17: IFF INDUCTIVE IN RF OUT



2.4 IFF Opcodes

TABLE 2-4: LIST OF OPCODES USED DURING TRANSPONDER OPERATION

Operational Code	Response
00000	Reserved for programming - EEPROM ERASE and FEEDBACK
00001	Write Configuration word
00010	Write to LSB of Serial Number (SER0)
00011	Write to MSB of Serial Number (SER1)
00100	Write 16-bits to USR0 in EEPROM
00101	Write 16-bits to USR1 in EEPROM
00110	Write 16-bits to USR2 in EEPROM
00111	Write 16-bits to USR3 in EEPROM
01000	Select encoder (Anticollision)
01001	Read 16-bit Configuration Word
01010	Read LSB Serial Number (SER0) 1 x 16-bit response
01011	Read MSB Serial Number (SER1) 1 x 16-bit response
01100	Read USR0
01101	Read USR1
01110	Read USR2
01111	Read USR3
11000	IFF1 32-bit challenge and response using key-1 and IFF algorithm 1
11001	IFF1 32-bit challenge and response using key-1 and IFF algorithm 2
11100	IFF2 32-bit challenge and response using key-2 and IFF algorithm 1
11101	IFF2 32-bit challenge and response using key-2 and IFF algorithm 2

Note: Dark shaded areas indicate operations only allowed when the HCS410 is in 2-key IFF mode.

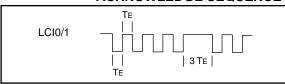
© 1997 Microchip Technology Inc. Preliminary DS40158B-page 15

2.5 IFF Special Features

2.5.1 ANTI-COLLISION

When the ACOL bit is set in the configuration word, anti-collision mode is entered. The HCS410 will start sending ACK pulses when it enters a magnetic field. The ACK pulses will stop as soon as the HCS410 detects a start bit from the decoder. A 'select encoder' opcode (01000) is then sent out by the decoder, followed by a 32-bit serial number. If the serial number matches the HCS410 serial number, the HCS410 will acknowledge with the acknowledge sequence as shown in Figure 2-18, A normal opcode for READ/WRITE will then be expected. If it does not match, the IFF encoder will stop transmitting ACK pulses until it is either removed from the field or the correct serial number is given.

FIGURE 2-18: SERIAL NUMBER CORRECT
ACKNOWLEDGE SEQUENCE



2.5.2 TRANSPONDER IN/RF OUT

When in transponder mode with ACOLI and XPRF set, the outputs of the HCS410's LC0:LC1 pins are echoed on the PWM output line. After transmitting the data on the LC pins, the data is then transmitted on the PWM line. The transmission format mirrors a code hopping transmission. The response replaces the 32-bit code hopping portion of the transmission. If the response is a 16-bit response, the 16 bits are duplicated to make up the 32-bit code hopping portion. The preamble, serial number, CRC, and queuing bits are all transmitted as normal (Figure 2-17).

This feature will be used in applications which use RF for long distance unidirectional authentication and short distance IFF.

3.0 EEPROM ORGANIZATION AND CONFIGURATION

The HCS410 has nonvolatile EEPROM memory which is used to store user programmable options. This information includes encoder keys, serial number, and up to 64-bits of user information.

The HCS410 has two modes in which it operates as specified by the configuration word. In the first mode the HCS410 has a single encoder key which is used for encrypting the code hopping portion of a CH Mode transmission and generating a response during IFF validation. Seed transmissions are allowed in this mode. In the second mode the HCS410 is a transponder device with two encoder keys.

The two different operating modes of the HCS410 lead to different EEPROM memory maps.

In IFF1 mode, the HCS410 can act as a code hopping encoder with Seed transmission, and as an IFF token with one key.

IFF1 Mode
64-bit Encoder Key 1
60-bit Seed
(SEED0, SEED1, SEED2, SEED3)
32-bit Serial Number
(SER0, SER1)
64-bit User Area
(USR0, USR1, USER2, USR3)
12-bit Discrimination Value and Overflow Bits.
16-bit Synchronization Counter
Configuration Data

In IFF2 mode, the HCS410 is able to act as a code hopping transmitter and an IFF token with two encoder keys.

IFF2 Mode					
64-bit Encoder Key 1					
64-bit Encoder Key 2					
32-bit Serial Number					
(SER0, SER1)					
64-bit User EEPROM					
(USR0, USR1, USER2, USR3)					
12-bit Discrimination Value and Overflow Bits.					
16-bit Synchronization Counter					
Configuration Data					

3.1 Encoder Key 1 and 2

The 64-bit encoder key1 is used by the transmitter to create the encrypted message transmitted to the receiver in Code Hopping Mode. An IFF operation, can use encoder key1 or key2 to generate the response to a challenge received. The key(s) is created and programmed at the time of production using a key generation algorithm. Inputs to the key generation algorithm are the serial number or seed for the particular transmitter being used and a secret manufacturer's code. While a number of key generation algorithms are supplied by Microchip, a user may elect to create their own method of key generation. This may be done providing that the decoder is programmed with the same means of creating the key for decryption purposes. If a seed is used (CH Mode), the seed will also form part of the input to the key generation algorithm.

3.2 Discrimination Value and Overflow

The discrimination value forms part of the code hopping portion of a code hopping transmission. The least significant 10 bits of the discrimination value are typically set to the least significant bits of the serial number. The most significant 2 bits of the discrimination value are the overflow bits (OVR1: OVR0). These are used to extend the range of the synchronization counter. When the synchronization counter wraps from FFFF₁₆ to 0000₁₆ OVR0 is cleared and the second time a wrap occurs OVR1 is cleared.

Once cleared, the overflow bits cannot be set again, thereby creating a permanent record of the counter overflow.

3.3 16-bit Synchronization Counter

This is the 16-bit synchronization counter value that is used to create the code hopping portion for transmission. This value will be changed after every transmission. The synchronization counter is not used in IFF mode.

3.4 60-bit Seed Word

This is the 60-bit seed code that will be transmitted when seed transmission is selected. This allows the system designer to implement the secure learn feature or use this fixed code word as part of a different key generation/tracking process or purely as a fixed code transmission. The seed is not available in IFF2-mode. A Seed transmission can be initiated in two ways, depending on the button inputs (Figure 3-1)

Seed transmission is available for function codes (Table 2-1) S[2:0] = 111 and S[2:0] = 011 (delayed). The delayed seed transmission starts with a normal code hopping transmission being transmitted for 3 seconds, before switching to a seed transmission. The two seed transmissions are shown in Figure 3-1.

Note: If both SEED and TMPSD are set, IFF2 mode is enabled.

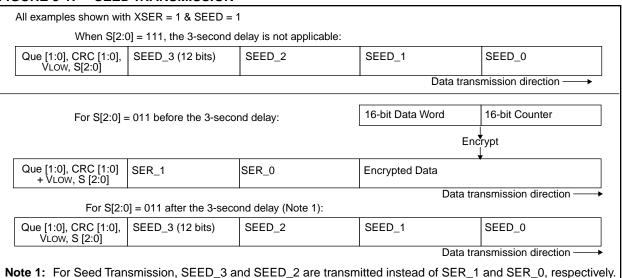
3.5 Encoder Serial Number

There are 32 bits allocated for the serial number and a selectable configuration bit (XSER) determines whether 32 or 28 bits will be transmitted. The serial number is meant to be unique for every transmitter.

3.6 User Data

The user EEPROM can be reprogrammed and read at any time using the IFF interface.

FIGURE 3-1: SEED TRANSMISSION



3.7 Configuration Data

The configuration data is used to select various encoder options. Further explanations of each of the bits are described in the following sections.

TABLE 3-1: CONFIGURATION OPTIONS SEED

Symbol	Description
CWBE	Code Word Blanking Enable
DAMP	Additional Damping on the LC Tank
SEED/ IFF2	Enable Seed Transmissions
TMPSD/ IFF2	Temporary Seed Transmissions
OSC0:3	Onboard Oscillator Tuning Bits
MTX3	Minimum 3 Code Words Transmitted
VLOW	Low Voltage Trip Point Selection
LED	Enable LED output
BSL0:1	Baudrate Select
PPM	Pulse Position Modulation
MANCH	Manchester Modulation Mode
ACOLI	Anti Collision Communication Enable
XPRF	Passive Proximity Activation
DINC	Delayed Increment Enable
XSER	Extended Serial Number

3.7.1 **CWBE:** CODE WORD BLANKING ENABLE AND **BSL:** BAUD RATE SELECT

Selecting this option allows code blanking as shown in Table 3-3. If this option is not selected, all code words are transmitted.

3.7.2 **DAMP:** LC TANK DAMPING

If DAMP = 1 additional damping is added to the LC tank allowing faster communication.

3.7.3 **SEED, TMPSD:** SEED TRANSMISSION

SEED	TMPSD	Description
0	0	No Seed
0	1	Seed Limited
1	0	Always Enabled
1	1	IFF2/No Seed

3.7.4 OSC: OSCILLATOR TUNING BITS

These bits allow the onboard oscillator to be tuned to within 10% of the nominal oscillator speed over both temperature and voltage.

TABLE 3-2: OSCILLATOR TUNING

osc	Description
1000	Fastest
1001	
1010	
•	Faster
•	i dotti
•	
1111	
0000	Nominal
0001	
0010	
•	Slower
•	Slower
•	
0110	
0111	Slowest

TABLE 3-3: BAUD RATE SELECTION

		Code Ho	pping Transmiss	Transponder Communication (TE)	
BSL 1	BSL 0	PWM [†]	Manchester	Codes Word Transmitted*	PPM
0	0	400 μs	800 μs	All	200 μs
0	1	200 μs	400 μs	1 of 2	200 μs
1	0	200 μs	400 μs	1 of 2	200 μs
1	1	100 μs	200 μs	1 of 4	100 μs

[†]Also transponder responses, if ACOLI and XPRF are set.

^{*}If code word blanking is enabled.

3.7.5 MTX3: MINIMUM CODE WORDS COMPLETED

If this bit is set, the HCS410 will transmit a minimum of 3 words before it powers itself down. If this bit is cleared, the HCS410 will only complete the current transmission. This feature will only work if VDD is connected directly to the battery as shown in Figure 2-1.

3.7.6 VLow: LOW VOLTAGE TRIP POINT

The low voltage trip point select bit is used to tell the HCS410 what VDD level is being used. This information will be used by the device to determine when to send the voltage low signal to the receiver. When this bit is set, the VDD level is assumed to be operating from a 5 volt or 6 volt supply. If the bit is cleared, then the VDD level is assumed to be 3.0 volts. Refer to Figure 5-3 for voltage trip point. When the battery reaches the VLOW point, the LED will not switch on during a code hopping transmission.

3.7.7 **LED: OUTPUT ENABLE**

If this bit is set in the configuration word the S2 line doubles as an LED output line. The LED output is driven high while the HCS410 is transmitting. If the bit is clear the S2/LED input is only used as an input and no output on the LED line is given. If the VDD drops below the point set by the VLOW bit the LED will indicate this by not switching on. The LED output operates with a 25 ms on and a 480 ms off duty cycle. The output first goes active 250 ms after the button debounce time expires.

3.7.8 **PPM:** PULSE POSITION MODULATION

When used in Transponder mode the communication from the transponder to the base can be either pulse position modulated or pulse width modulated as in a normal transmission. A '1' selects PPM and a '0' selects PWM Modulation.

3.7.9 **MANCH:** MANCHESTER CODE ENCODING

MANCH selects between Manchester code modulation and PWM modulation in code hopping mode. If MANCH = 1, Manchester code modulation is selected. If MANCH is cleared, PWM modulation is selected.

3.7.10 ACOLI: ANTI-COLLISION COMMUNICATION AND XPRF: TRANSPONDER ECHOING ON PWM OUTPUT

If ACOLI is set the anti-collision operation during bidirectional transponder mode (IFF) is enabled. This feature is useful in situations where multiple transponders enter the magnetic field simultaneously.

If XPRF is set, and ACOLI is cleared, the HCS410 starts sending out ACK pulses when it detects a magnetic field. If the HCS410 doesn't receive a start bit from the decoder within 100 ms, the HCS410 will transmit a code hopping transmission on LC and PWM pins for 2 seconds

If both the ACOLI and XPRF are set, all of the HCS410 transponder responses are echoed on the PWM output, as described in Section 2.5.1.

3.7.11 *DINC: DELAYED INCREMENT

If this bit is set the HCS410 increments the counter by 12, 20 seconds after the last button press occurred. This is only canceled if another press occurs before the 20 seconds expires. Systems that use this feature will circumvent the latest jamming-code grabbing attackers.

3.7.12 XSER: EXTENDED SERIAL NUMBER

If XSER is set, the full 32-bit serial number is transmitted. If XSER is cleared, the four most significant bits of the serial number are substituted by S[2:0] = S2:S1:S0: 0 and is compatible with the HCS200/300/301.

*Patents have been applied for.

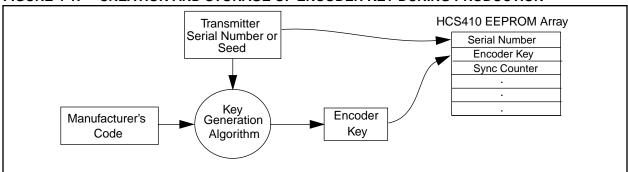
4.0 INTEGRATING THE HCS410 INTO A SYSTEM

Use of the HCS410 in a system requires a compatible decoder. This decoder is typically a microcontroller with compatible firmware. Firmware routines that accept transmissions from the HCS410, decrypt the code hopping portion of the data stream and perform IFF functions are available. These routines provide system designers the means to develop their own decoding system.

4.1 Key Generation

The serial number for each transmitter is programmed by the manufacturer at the time of production. The generation of the encoder key is done using a key generation algorithm (Figure 4-1). Typically, inputs to the key generation algorithm are the serial number of the transmitter or seed value, and a 64-bit manufacturer's code. The manufacturer's code is chosen by the system manufacturer and must be carefully controlled. The manufacturer's code is a pivotal part of the overall system security.

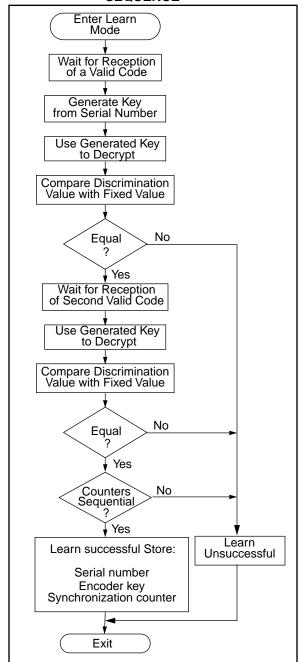
FIGURE 4-1: CREATION AND STORAGE OF ENCODER KEY DURING PRODUCTION



4.2 <u>Learning an HCS410 to a Receiver</u>

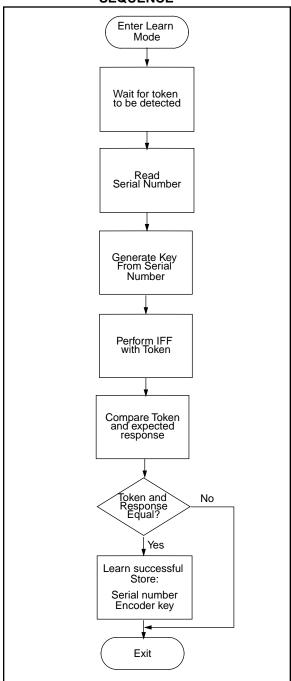
In order for a transmitter to be used with a decoder, the transmitter must first be 'learned'. Several learning strategies can be followed in the decoder implementation. When a transmitter is learned to a decoder, it is suggested that the decoder stores the serial number and current synchronization counter value (synchronization counter stored in CH Mode only) in EEPROM. The decoder must keep track of these values for every transmitter that is learned (Figure 4-2 and Figure 4-3).

FIGURE 4-2: TYPICAL CH MODE LEARN SEQUENCE



The maximum number of transmitters that can be learned is only a function of how much EEPROM memory storage is available. The decoder must also store the manufacturer's code in order to learn an HCS410, although this value will not change in a typical system so it is usually stored as part of the microcontroller ROM code. Storing the manufacturer's code as part of the ROM code is also better for security reasons.

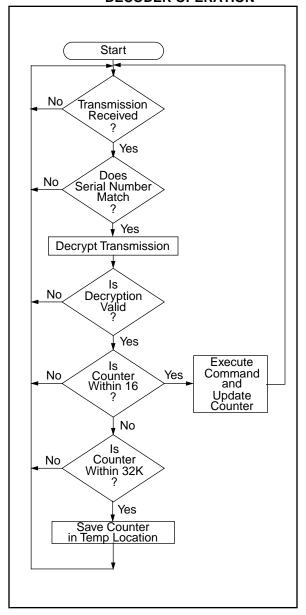
FIGURE 4-3: TYPICAL IFF LEARN SEQUENCE



4.3 CH Mode Decoder Operation

In a typical decoder operation (Figure 4-4), the key generation on the decoder side is done by taking the serial number from a transmission and combining that with the manufacturer's code to create the same encoder key that is stored in the HCS410. Once the encoder key is obtained, the rest of the transmission can be decrypted. The decoder waits for a transmission and immediately checks the serial number to determine if it is a learned transmitter. If it is, the code hopping portion of the transmission is decrypted using the stored key. It uses the discrimination bits to determine if the decryption was valid. If everything up to this point is valid, the synchronization counter value is evaluated.

FIGURE 4-4: TYPICAL CH MODE DECODER OPERATION



4.3.1 SYNCHRONIZATION WITH DECODER

The KEELOQ technology features a sophisticated synchronization technique (Figure 4-5) which does not require the calculation and storage of future codes. If the stored counter value for that particular transmitter and the counter value that was just decrypted are within a window of say 16, the counter is stored and the command is executed. If the counter value was not within the single operation window, but is within the double operation window of say 32K window, the transmitted synchronization counter value is stored in temporary location and it goes back to waiting for another transmission. When the next valid transmission is received. it will compare the new value with the one in temporary storage. If the two values are sequential, it is assumed that the counter had just gotten out of the single operation 'window', but is now back in sync, so the new synchronization counter value is stored and the command executed. If a transmitter has somehow gotten out of the double operation window, the transmitter will not work and must be relearned. Since the entire window rotates after each valid transmission, codes that have

been used are part of the 'blocked' (32K) codes and are no longer valid. This eliminates the possibility of grabbing a previous code and retransmitting to gain entry.

> The synchronization method described in this section is only a typical implementation and because it is usually implemented in firmware, it can be altered to fit the needs of a particular system

FIGURE 4-5: SYNCHRONIZATION WINDOW

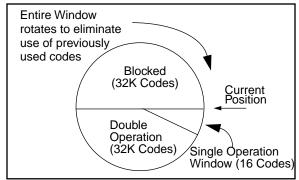
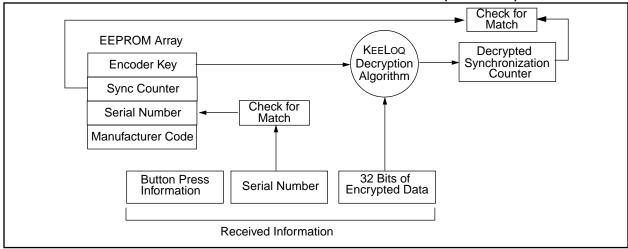


FIGURE 4-6: BASIC OPERATION OF A CODE HOPPING RECEIVER (DECODER)



© 1997 Microchip Technology Inc. Preliminary DS40158B-page 23

4.4 IFF Decoder Operation

In a typical IFF decoder, the key generation on the decoder side is done by reading the serial number from a token and combining that with the manufacturer's code to recreate the encoder key that is stored on the token. The decoder polls for the presence of a token. Once detected the decoder reads the serial number. If the token has been learned, the decoder sends a challenge and reads the token's response. The decoder uses the encoder key stored in EEPROM and generates an expected response to the challenge. The token's response is compared to the expected response. If the responses match the appropriate output is activated.

FIGURE 4-7: TYPICAL IFF DECODER OPERATION

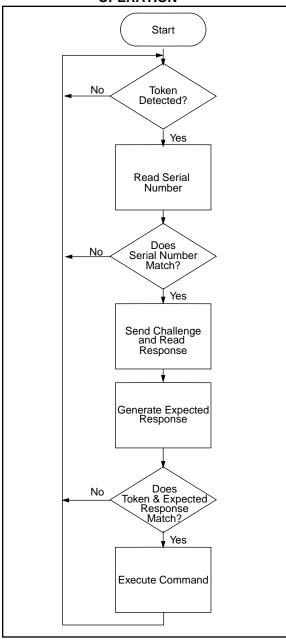
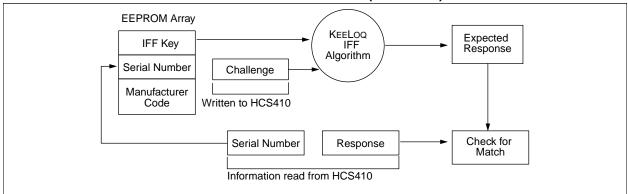


FIGURE 4-8: BASIC OPERATION OF AN IFF RECEIVER (DECODER)



5.0 ELECTRICAL CHARACTERISTICS

TABLE 5-1: ABSOLUTE MAXIMUM RATING

Symbol	Item	Rating	Units
VDD	Supply voltage	-0.3 to 6.6	V
Vin*	Input voltage	-0.3 to VDD + 0.3	V
Vout	Output voltage	-0.3 to VDD + 0.3	V
lout	Max output current	50	mA
Tstg	Storage temperature	-55 to +125	C (Note)
TLSOL	Lead soldering temp	300	C (Note)
VESD	ESD rating	4000	V

Note: Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent damage to the device.

* If a battery is inserted in reverse, the protection circuitry switches on, protecting the device and draining the battery.

TABLE 5-2: DC AND TRANSPONDER CHARACTERISTICS

Commercial (C): Tamb = 0° C to 70° C Industrial (I): Tamb = -40° C to 85° C

industriai (i): Tamb = -2	10°C to 85°C	<i>-</i>				
		2.0V < VDD < 6.3V				
Parameter	Symbol	Min	Typ ¹	Max	Unit	Conditions
Average operating current ²	IDD (avg)		0.1 0.5	1.4	mA	VDD = 3.0V VDD = 6.3V
Programming current	IDDP		2.2	3.5	mA	
Standby current	IDDS		10	1000	nA	
High level input voltage	ViH	1.3		VDD + 0.3	V	0.8 + 0.25 VDD
Low level input voltage	VIL	-0.3		0.15 VDD	V	
High level output voltage	Voн	0.7 VDD 0.7 VDD			V	VDD = 2V, IOH =- 1 mA VDD=6.3V, IOH,= -5 mA
Low level output voltage	Vol			0.08 VDD 0.08 VDD	V	VDD = 2V, IOH =1mA VDD = 6.3V,IOH = 5mA
LED output current	ILED	1.5	2.5		mA	VDD = 2.0V, VLED = 1.5V
Switch input resistor	RS		60		kW	
PWM input resistor	RPWM		120		kW	
LC input current	ILC			10.0	mA	VLCC=15 VP-P
LC input clamp voltage	VLCC		15		V	ILC <10 mA
LC induced output current	Vddi			8.0	mA	
LC induced output voltage	VDDV		6.7		V	7.5 VP-P < VLCC < 15 VP-P
Carrier frequency	fc		125		kHz	
External LC Inductor value	L		900		μН	
External LC Capacitor value	С		1.8		pF	

Note 1: Typical values at 25°C.

2: No load connected.

3: LC inputs are clamped at 15 volts.

© 1997 Microchip Technology Inc. Preliminary DS40158B-page 25

FIGURE 5-1: POWER UP AND TRANSMIT TIMING

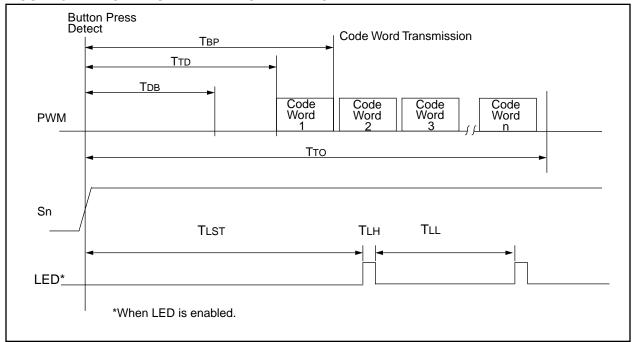


TABLE 5-3: POWER UP AND TRANSMIT TIMING REQUIREMENTS

VDD = +2.0 to 6.3V Commercial (C):Tamb = 0° C to +70°C

Industrial (I): Tamb = -40° C to $+85^{\circ}$ C

Parameter	Symbol	Min	Тур.	Max	Unit	Remarks
Time to second button press	Твр	34 + Code Word Time	38 + Code Word Time	42 + Code Word Time	ms	(Note 1)
Transmit delay from button detect	TTD	34.2	38	41.8	ms	(Note 2)
Debounce delay	TDB	27	30	33	ms	
Auto-shutoff time-out period	Тто	18	20	22	S	(Note 3)
Time to first LED on	TLST		200		ms	
LED high-time	TLH		25		ms	
LED low-time	TLL		480		ms	

Note 1: TBP is the time in which a second button can be pressed without completion of the first code word and the intention was to press the combination of buttons.

- 2: Transmit delay maximum value if the previous transmission was successfully transmitted.
- **3:** The auto-shutoff timeout period is not tested.

Temperature °C

Values are for calibrated oscillator.

10 20 30 40 50 60 70 80 90

FIGURE 5-2: HCS410 NORMALIZED TE VS. TEMP

TABLE 5-4: CODE WORD TRANSMISSION TIMING PARAMETERS—PWM MODE

-50 -40 -30 -20 -10 0

Note:

VDD = +2.0	Code Words Transmitted										
Commercial (C): Tamb = 0° C to $+70^{\circ}$ C Industrial (I): Tamb = -40° C to $+85^{\circ}$ C			BSL1 = 0, BSL0 = 0				BSL1 = 0, BSL0 = 1				
Symbol	Characteristic	Number of TE	Min.	Тур.	Max.	Number of TE	Min.	Тур.	Max.	Units	
TE	Basic pulse element	1	360	400	440	1	180.0	200.0	220.0	ms	
Твр	PWM bit pulse width	3	1080	1200	1320	3	540.0	600.0	660.0	ms	
ТР	Preamble duration	32	12	12.8	14	32	5.76	6.0	7.04	ms	
Тн	Header duration	10	4	4.0	4	10	1.80	2.0	2.20	ms	
Тнор	Code hopping duration	96	35	38.4	42	96	17.28	19.20	21.12	ms	
TFIX	Fixed code duration	111	39.96	44.4	48.84	111	19.98	22.20	24.42	ms	
TG	Guard time	46	16.6	18.4	20.2	46	8.3	9.6	10.1	ms	
_	Total transmit time	295	106.2	118.0	129.8	295	53.1	59.0	64.9	ms	

 $\textbf{Note:} \ \ \, \textbf{The timing parameters are not tested but derived from the oscillator clock}.$

VDD = +2.0	Code Words Transmitted									
Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			BSL1 = 1, BSL0 = 0				BSL1 = 0, BSL0 = 1			
Symbol	Characteristic	Number of TE	Min.	Тур.	Max.	Number of TE	Min.	Тур.	Max.	Units
TE	Basic pulse element	1	180.0	200.0	220.0	1	90.0	100.0	110.0	ms
Твр	PWM bit pulse width	3	540.0	600.0	660.0	3	270.0	300.0	330.0	ms
ТР	Preamble duration	32	5.76	6.0	7.04	32	2.88	3.0	3.52	ms
Тн	Header duration	10	1.80	2.0	2.20	10	0.90	1.0	1.10	ms
Тнор	Code hopping duration	96	17.28	19.20	21.12	96	8.64	9.60	10.56	ms
TFIX	Fixed code duration	111	19.98	22.2	24.42	111	9.99	11.1	12.21	ms
Tg	Guard time	46	8.3	9.6	10.1	46	41	4.6	5.1	ms
_	Total transmit time	295	53.1	59.0	64.9	295	26.6	29.5	32.5	ms

Note: The timing parameters are not tested but derived from the oscillator clock.

TABLE 5-5: CODE WORD TRANSMISSION TIMING PARAMETERS—MANCHESTER MODE

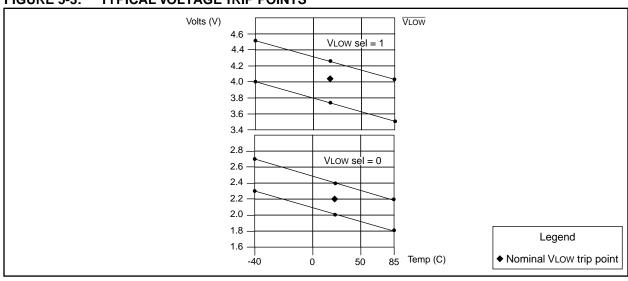
VDD = +2.0V to 6.3V				Code Words Transmitted									
Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			BSL1 = 0, BSL0 = 0				BSL1 = 0, BSL0 = 1						
Symbol	Characteristic	Number of TE	Min.	Тур.	Max.	Number of TE	Min.	Тур.	Max.	Units			
TE	Basic pulse element	1	720.0	800.0	880.0	1.0	360.0	400.0	440.0	ms			
ТР	Preamble duration	32	23.04	25.60	28.16	32.0	11.52	12.80	14.08	ms			
Тн	Header duration	4	2.88	3.20	3.52	4.0	1.44	1.60	1.76	ms			
TSTART	Start bit	2	1.44	1.60	1.76	2.0	0.72	0.80	0.88	ms			
Тнор	Code hopping duration	64	46.08	51.20	56.32	64.0	23.04	25.60	28.16	ms			
TFIX	Fixed code duration	74	53.28	59.20	65.12	74	26.64	29.60	32.56	ms			
Тѕтор	Stop bit	2	1.44	1.60	1.76	2.0	0.72	0.80	0.88	ms			
TG	Guard time	32	23.0	25.6	28.2	32	11.5	12.8	14.1	ms			
_	Total transmit time	210	151.2	168	184.8	210	75.6	84.0	92.4	ms			

Note: The timing parameters are not tested but derived from the oscillator clock.

VDD = +2.0V to 6.3V				Code Words Transmitted									
Commercial (C): Tamb = 0°C to +70°C Industrial (I): Tamb = -40°C to +85°C			BSL1 = 1, BSL0 = 0				BSL1 = 1, BSL0 = 1						
Symbol	Characteristic	Number of TE	Min.	Тур.	Max.	Number of TE	Min.	Тур.	Max.	Units			
TE	Basic pulse element	1	360.0	400.0	440.0	1.0	180.0	200.0	220.0	ms			
ТР	Preamble duration	32	11.52	12.80	14.08	32.0	5.76	6.40	7.04	ms			
Тн	Header duration	4	1.44	1.60	1.76	4.0	0.72	0.80	0.88	ms			
TSTART	Start bit	2	0.72	0.80	0.88	2.0	0.36	0.40	0.44	ms			
Тнор	Code hopping duration	64	23.04	25.60	28.16	64.0	11.52	12.80	14.08	ms			
TFIX	Fixed code duration	74	26.64	29.60	32.56	74	13.32	14.8	16.28	ms			
Тѕтор	Stop bit	2.0	0.72	0.80	0.88	2.0	0.36	0.40	0.44	ms			
Tg	Guard time	32	11.5	12.8	14.1	32	5.8	6.4	7.0	ms			
	Total transmit time	210	75.6	84.0	92.4	210	37.8	42.0	46.2	ms			

Note: The timing parameters are not tested but derived from the oscillator clock.

FIGURE 5-3: TYPICAL VOLTAGE TRIP POINTS



NOTES:

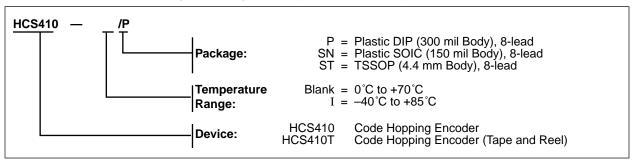
© 1997 Microchip Technology Inc. Preliminary DS40158B-page 29



NOTES:

HCS410 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.



Sales and Support

Data Sheets

Products supported by a preliminary Data Sheet may have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

- 1. Your local Microchip sales office.
- 2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277.
- 3. The Microchip's Bulletin Board, via your local CompuServe number (CompuServe membership NOT required).

© 1997 Microchip Technology Inc. Preliminary DS40158B-page 31



WORLDWIDE SALES & SERVICE

AMERICAS

Corporate Office

Microchip Technology Inc. 2355 West Chandler Blvd. Chandler, AZ 85224-6199 Tel: 602-786-7200 Fax: 602-786-7277 Technical Support: 602 786-7627 Web: www.microchip.com

Atlanta

Microchip Technology Inc. 500 Sugar Mill Road, Suite 200B Atlanta, GA 30350 Tel: 770-640-0034 Fax: 770-640-0307

Boston

Microchip Technology Inc. 5 Mount Royal Avenue Marlborough, MA 01752 Tel: 508-480-9990 Fax: 508-480-8575

Chicago

Microchip Technology Inc. 333 Pierce Road, Suite 180 Itasca, IL 60143 Tel: 630-285-0071 Fax: 630-285-0075

Dallas

Microchip Technology Inc. 14651 Dallas Parkway. Suite 816 Dallas, TX 75240-8809 Tel: 972-991-7177 Fax: 972-991-8588

Dayton

Microchip Technology Inc. Two Prestige Place, Suite 150 Miamisburg, OH 45342 Tel: 937-291-1654 Fax: 937-291-9175

Los Angeles

Microchip Technology Inc. 18201 Von Karman, Suite 1090 Irvine, CA 92612 Tel: 714-263-1888 Fax: 714-263-1338

New York

Microchip Technology Inc. 150 Motor Parkway, Suite 416 Hauppauge, NY 11788 Tel: 516-273-5305 Fax: 516-273-5335

San Jose

Microchip Technology Inc. 2107 North First Street, Suite 590 San Jose, CA 95131 Tel: 408-436-7950 Fax: 408-436-7955

Toronto

Microchip Technology Inc. 5925 Airport Road, Suite 200 Mississauga, Ontario L4V 1W1. Canada Tel: 905-405-6279 Fax: 905-405-6253

ASIA/PACIFIC

Hong Kong

Microchip Asia Pacific RM 3801B, Tower Two Metroplaza 223 Hing Fong Road Kwai Fong, N.T., Hong Kong Tel: 852-2-401-1200 Fax: 852-2-401-3431

Microchip Technology India No. 6, Legacy, Convent Road Bangalore 560 025, India Tel: 91-80-229-0061 Fax: 91-80-229-0062

Korea

Microchip Technology Korea 168-1, Youngbo Bldg. 3 Floor Samsung-Dong, Kangnam-Ku Seoul, Korea Tel: 82-2-554-7200 Fax: 82-2-558-5934

Shanghai

Microchip Technology RM 406 Shanghai Golden Bridge Bldg. 2077 Yan'an Road West, Hongiao District Shanghai, PRC 200335 Tel: 86-21-6275-5700 Fax: 86 21-6275-5060

Singapore

Microchip Technology Taiwan Singapore Branch 200 Middle Road #10-03 Prime Centre Singapore 188980 Tel: 65-334-8870 Fax: 65-334-8850

Taiwan, R.O.C

Microchip Technology Taiwan 10F-1C 207 Tung Hua North Road Taipei, Taiwan, ROC Tel: 886 2-717-7175 Fax: 886-2-545-0139

EUROPE

United Kingdom

Arizona Microchip Technology Ltd. Unit 6, The Courtyard Meadow Bank, Furlong Road Bourne End, Buckinghamshire SL8 5AJ Tel: 44-1628-851077 Fax: 44-1628-850259

Arizona Microchip Technology SARL Zone Industrielle de la Bonde 2 Rue du Buisson aux Fraises 91300 Massy, France Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Arizona Microchip Technology GmbH Gustav-Heinemann-Ring 125 D-81739 Müchen, Germany Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Arizona Microchip Technology SRL Centro Direzionale Colleone Palazzo Taurus 1 V. Le Colleoni 1 20041 Agrate Brianza Milan, Italy Tel: 39-39-6899939 Fax: 39-39-6899883

JAPAN

Microchip Technology Intl. Inc. Benex S-1 6F 3-18-20, Shin Yokohama Kohoku-Ku, Yokohama Kanagawa 222 Japan Tel: 81-4-5471- 6166 Fax: 81-4-5471-6122

06/16/97

All rights reserved. ©1997, Microchip Technology Incorporated, USA. 7/97



Printed on recycled paper.

Information contained in this publication regarding device applications and the like is intended for suggestion only and may be superseded by updates. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights. The Microchip logo and name are registered trademarks of Microchip Technology Inc. in the U.S.A. and other countries. All rights reserved. All other trademarks mentioned herein are the property of their respective companies.